REMARKS

Examiner J. Diaz is thanked for a complete search and thorough Office Action.

Response dated January 30, 2003 to previous Office Action dated December 3, 2002 is still valid. The Examiner's Remarks for rejecting the applicant's claimed invention are flawed as detailed in our reply below.

Reconsideration of the rejection of claims 18-19 under 35 U.S.C. 102(e) as being anticipated by Saitou et al., U.S. Patent No. 5,739,546, is respectfully requested for the following reasons.

The prior art (Saitou et al.) refers to a metal test structure that is formed partially in the kerf area. Not only is the test structure formed in the kerf area, but Saitou makes two metal test lines with an insulating layer between them: one metal line is a power supply line, and the other is a ground line. On the other hand, the applicant's fill layer (is limited) to the kerf area, and (does not extend into the chip area) as does Saitou's test line structure. The prior art is quite different from the applicant's single layer fill structure.

where
where

REPLY TO EXAMINER'S RESPONSE TO ARGUMENTS

Below is a detailed reply to th Examiner's Response to Arguments in Office Action dated 04/24/2003. On page 4, line 6 -9, the Examiner states "Thus, the patterned conductive layer (6) of Saitou et al. is a 'patterned fill layer' since the patterned conductive layer (6) is formed in the kerf areas and is formed of the same metal material as the patterned conductive layer formed in the semiconductor region."

Saitou's invention does not refer to a "fill layer" or a "patterned fill layer" but refers to ground line conductor 6 (col. 5, lines 35-38) for testing. This line 6 is not used as a fill layer. As clearly depicted in Saitou's Figs. 1-3, conducting line 6 only fills one-third of the kerf area. The Examiner can verify that Saitou's metal line 6 does not fill the kerf area 3 by using a ruler to measure the widths of line 6 and the kerf area 3 in Figs. 1 and 2. Saitou's structure fails to anticipate the applicant's structure. In the applicant's structure the spacing S, as shown in Figs. 6-7 and as claimed in claim 21, is much smaller than Saitou's spacing between the test line and the edge of the chip area. Therefore, Saitou's narrow conducting line 6 would not achieve the applicant's claimed invention for forming a structure with a planar insulating surface at the corner of the chip (die) area.

The Examiner also states on page 4, starting on line 10: "With regards to the planar silicon oxide layer, the Examiner disagrees with Applicant. Saitou et al. teaches a silicon oxide layer (7) formed on the patterned fill layer (6) (see Figure 2). After a carefully review of the drawings, the Examiner concluded that Figure 3, which is a cross sectional view of Figure 1, further provides the teaching of a planar layer, as required by Applicant. Figure 3 shows that, the silicon oxide layer (7) is planar over the surface of the patterned fill layer (6). Consequently, the reference Saitou et al. anticipated the claimed limitation since Saitou et al. teach a planar silicon oxide layer formed over the patterned fill layer."

It is not clear how the Examiner concludes from Saitou's Fig. 3 that layer 7 over the conducting line 6 is a planar layer. If the Examiner will take a ruler and align it with the top surface of layer 7 in Saitou's Fig. 2 or 3, it is clear that layer 7 is not planar over the metal test line 6. Saitou's layer 7 is more likely a conformal layer. Saitou et al. do not describe the deposition method of layer 7. Layer 7 appears to be chemical-vapor deposited SiO_2, which would deposit conformally over the conducting test line 6. The applicant's invention is a fill structure for forming a spin-on planar glass layer over the fill layers in the kerf area with narrow spacings S between the fill layer and the edge of the chip on the substrate.

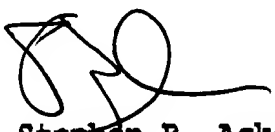
The Examiner states that Saitou in column 6, lines 61-65 clearly anticipates the applicant's multilevel metal structure. Since Saitou's single-level metal test line structure in the first embodiment is non-planar, it is not possible for Saitou to achieve a multi-metal planar structure, and therefore, Saitou's multi-level structure would not result in the applicant's planar structure.

Reconsideration of the rejection of claim 20 under 35 U.S.C. 103(a) as being unpatentable over Saitou et al. (U.S. Patent 5,739,546) in view of Lou (U.S. Patent 5,759,906), and of claims 21-22 under 35 U.S.C. 103(a) as being unpatentable over Saitou et al. (U.S. patent 5,739,946) is respectfully requested for the following reasons.

Claims 20-22 are dependent claims that do not stand on their own merits but support independent claim 18.

It is requested that Examiner Jose R. Diaz call the undersigned Attorney at 845-452-5863 should there be anything that can be done to help bring this Patent Application to Allowance.

Respectfully submitted,



Stephen B. Ackerman

Reg. No. 37,761